TMS 4051 JL, NL
4096-BIT DYNAMIC RANDOM ACCESS MEMORIES

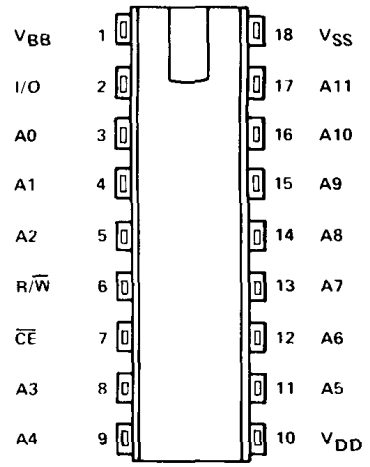
MOS LSI

- 4096 x 1 Organization
- 18-Pin 300-Mil Package Configuration
- Single Low-Capacitance TTL-Compatible Clock
- Multiplexed Data Input/Output
- 2 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4051	300 ns	470 ns	730 ns
TMS 4051-1	250 ns	430 ns	660 ns

- Full TTL Compatibility on All Inputs (No Pull-up Resistors Needed Except with $\overline{CE}$)
- Registers for Addresses Provided on Chip
- Open-Drain Output Buffer
- Low-Power Dissipation
  - 460 mW Operating (Typical)
  - 60 mW Standby (Typical)
- N-Channel Silicon-Gate Technology
- Refresh time: 2 ms or less

18-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



VDD +12V power supply
Vss 0V ground
VBB − 5V power supply

TMS 4060 JL, NL
4096-BIT DYNAMIC RANDOM-ACCESS MEMORIES

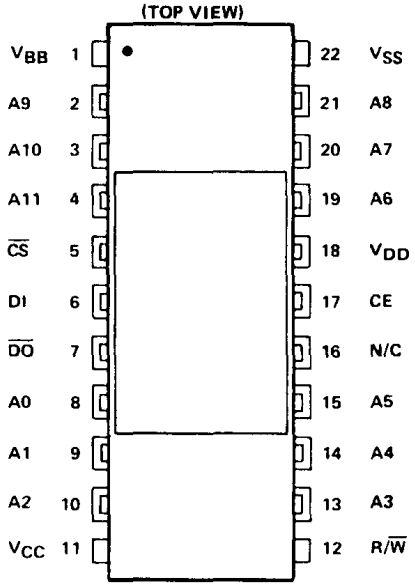
MOS LSI

- 4096 x 1 Organization
- 3 Performance Ranges:

	ACCESS TIME (MAX)	READ OR WRITE CYCLE (MIN)	READ, MODIFY WRITE CYCLE (MIN)
TMS 4060	300 ns	470 ns	710 ns
TMS 4060-1	250 ns	430 ns	640 ns
TMS 4060-2	200 ns	400 ns	580 ns

- Full TTL Compatibility on All Inputs Except CE (No Pull-Up Resistors Needed)
- Low Power Dissipation
  - 400 mW Operating (Typical)
  - 0.2 mW Standby (Typical)
- Single Low-Capacitance Clock
- N-Channel Silicon-Gate Technology
- 22-Pin 400-Mil Dual-in-Line Package
- Refresh time: 2 ms or less

22-PIN CERAMIC AND PLASTIC DUAL-IN-LINE PACKAGES (TOP VIEW)



Vcc + 5V power supply
Vss 0V ground
VDD +12V power supply
VBB − 5V power supply

4096 BIT DYNAMIC RAMS

DESCRIPTION

The μPD411A Family consists of four 4096 words by 1 bit dynamic N-channel MOS RAMs. They are designed for memory applications where very low cost and large bit storage are important design objectives. The μPD411A Family is designed using dynamic circuitry which reduces the standby power dissipation.

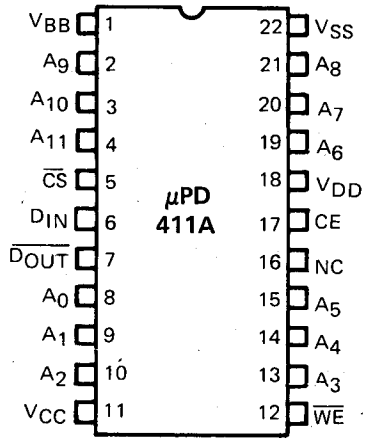
Reading information from the memory is non-destructive. Refreshing is easily accomplished by performing one read cycle on each of the 64 row addresses. Each row address must be refreshed every two milliseconds. The memory is refreshed whetl Chip Select is a logic high or a logic low.

FEATURES

- Low Standby Power
- 4096 words x 1 bit Organization
- A single low-capacitance high level clock input with solid ±1 volt margins.
- Inactive Power 0.7 mW (Typ.)
- Power Supply +12, +5, −5V
- Easy System Interface
- TTL Compatible (Except CE)
- Address Registers on the Chip
- Simple Memory Expansion by Chip Select
- Three State Output and TTL Compatible
- 22 pin Plastic or Cerdip Dual-in-Line Package
- Replacement for INTEL's 2107B, TI's 4060 and Equivalent Devices.
- 4 Performance Ranges:

	ACCESS TIME	R/W CYCLE	RMW CYCLE	REFRESH TIME
μPD411A-E	350 ns	800 ns	960 ns	1 ms
μPD411A	300 ns	470 ns	650 ns	2 ms
μPD411A-1	250 ns	430 ns	600 ns	2 ms
μPD411A-2	200 ns	400 ns	520 ns	2 ms

PIN CONFIGURATION



PIN NAMES

A_0 - A_{11}	Address Inputs
A_0 - A_5	Refresh Addresses
CE	Chip Enable
$\overline{CS}$	Chip Select
D_{IN}	Data Input
$\overline{D_{OUT}}$	Data Output
$\overline{WE}$	Write Enable
V_{DD}	Power (+12V)
V_{CC}	Power (+5V)
V_{SS}	Ground
V_{BB}	(Powe. −5V)
NC	No Connection

FUNCTIONAL DESCRIPTION

CE Chip Enable

A single external clock input is required. All read, write, refresh and read-modify-write operations take place when chip enable input is high. When the chip enable is low, the memory is in the low power standby mode. No read/write operations can take place because the chip is automatically precharging.

$\overline{CS}$ Chip Select

The chip select terminal affects the data in, data out and read/write inputs. The data input and data output terminals are enabled when chip select is low. The chip select input must be low on or before the rising edge of the chip enable and can be driven from standard TTL circuits. A register for the chip select input is provided on the chip to reduce overhead and simplify system design.

$\overline{WE}$ Write Enable

The read or write mode is selected through the write enable input. A logic high on the $\overline{WE}$ input selects the read mode and a logic low selects the write mode. The $\overline{WE}$ terminal can be driven from standard TTL circuits. The data input is disabled when the read mode is selected.

A_0–A_{11} Addresses

All addresses must be stable on or before the rising edge of the chip enable pulse. All address inputs can be driven from standard TTL circuits. Address registers are provided on the chip to reduce overhead and simplify system design.

D_{IN} Data Input

Data is written during a write or read-modify-write cycle while the chip enable is high. The data in terminal can be driven from standard TTL circuits. There is no register on the data in terminal.

$\overline{D_{OUT}}$ Data Output

The three state output buffer provides direct TTL compatibility with a fan-out of two TTL gates. The output is in the high-impedance (floating) state when the chip enable is low or when the Chip Select input is high. Data output is inverted from data in.

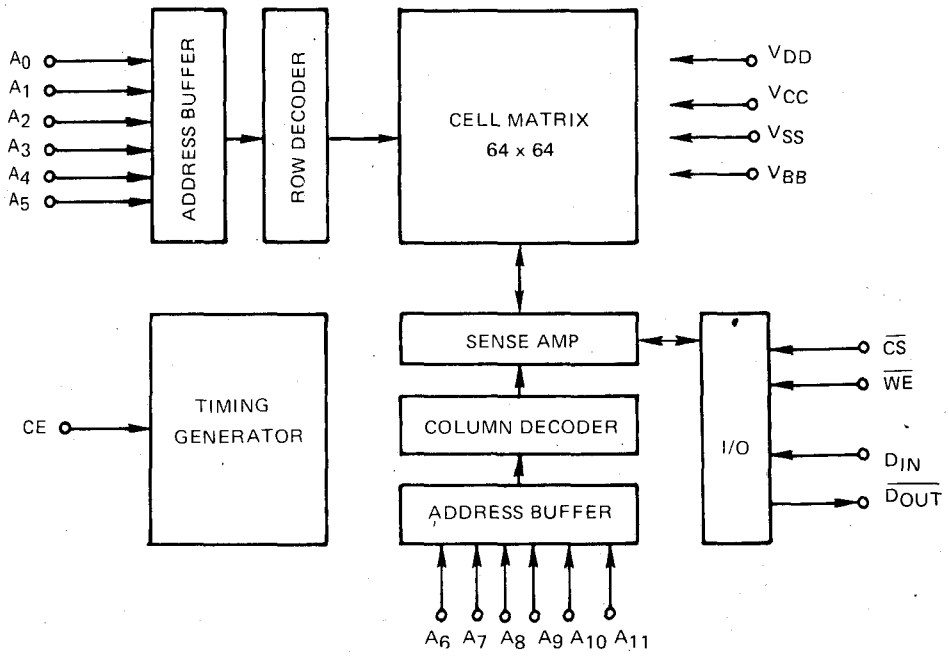
Refresh

Refresh must be performed every two milliseconds by cycling through the 64 addresses of the lower-order-address inputs A_0 through A_5 or by addressing every row within any 2*-millisecond period. Addressing any row refreshes all 64 bits in that row.

The chip does not need to be selected during the refresh. If the chip is refreshed during a write mode, the chip select must be high.

*μPD411A-E = 1 millisecond refresh period.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Operating Temperature	0°C to +70°C
Storage Temperature	−55°C to +150°C
Output Voltage ①	+20 to −0.3 Volts
All Input Voltages ①	+20 to −0.3 Volts
Supply Voltage V_{DD} ①	+20 to −0.3 Volts
Supply Voltage V_{CC} ①	+20 to −0.3 Volts
Supply Voltage V_{SS} ①	+20 to −0.3 Volts
Power Dissipation	1.0W

Note: ① Relative to V_{BB}.

COMMENT: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

*T_a = 25°C

DC CHARACTERISTICS

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP. ①	LIMITS MAX.	UNIT	TEST CONDITIONS
Input Load Current	I_{LI}		0.01	10	μA	V_{IN} = V_{IL} MIN to V_{IH} MAX
CE Input Load Current	I_{LC}		0.01	10	μA	V_{IN} = V_{ILC} MIN to V_{IHC} MAX
Output Leakage Current for High Impedance State	I_{LO}		0.01	±10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH} V_O = 0V to 5.25V
V_{DD} Supply Current during CE off	I_{DD} OFF		50	200	μA	CE = −1.0V to 0.6V
V_{DD} Supply Current during CE on	I_{DD} ON		35	50	mA	CE = V_{IHC}, T_a = 25°C
Average V_{DD} Current						T_a = 25°C
μPD411A-E	I_{DD} AV		25	40	mA	Cycle Time = 800 ns
μPD411A	I_{DD} AV		38	55	mA	Cycle Time = 470 ns
μPD411A-1	I_{DD} AV		38	55	mA	Cycle Time = 430 ns
μPD411A-2	I_{DD} AV		38	55	mA	Cycle Time = 400 ns
V_{BB} Supply Current ②	I_{BB}		5	100	μA	
V_{CC} Supply Current during CE off ③	I_{CC} OFF		0.01	10	μA	CE = V_{ILC} or $\overline{CS}$ = V_{IH}
Input Low Voltage	V_{IL}	−1.0		0.6	V	
Input High Voltage	V_{IH}	2.4		V_{CC} + 1	V	
CE Input Low Voltage	V_{ILC}	−1.0		0.6	V	
CE Input High Voltage	V_{IHC}	V_{DD} − 1	V_{DD}	V_{DD} + 1	V	
Output Low Voltage	V_{OL}	0		0.40	V	I_{OL} = 3.2 mA
Output High Voltage	V_{OH}	2.4		V_{CC}	V	I_{OH} = −2.0 mA

Notes: ① Typical values are for T_a = 25°C and nominal power supply voltages.
② The I_{BB} current is the sum of all leakage currents.
③ During CE on V_{CC} supply current is dependent on output loading.

CAPACITANCE

T_a = 0°C to 70°C, V_{DD} = +12V ± 10%, V_{CC} = +5V ± 10%, V_{BB} = −5V ± 10%, V_{SS} = 0V

PARAMETER	SYMBOL	LIMITS MIN.	LIMITS TYP.	LIMITS MAX.	UNIT	TEST CONDITIONS
Address Capacitance	C_{AD}			6	pF	V_{IN} = V_{SS}
$\overline{CS}$ Capacitance	C_{CS}			6	pF	V_{IN} = V_{SS}
D_{IN} Capacitance	C_{IN}			6	pF	V_{IN} = V_{SS}
$\overline{D_{OUT}}$ Capacitance	C_{OUT}			7	pF	V_{OUT} = V_{SS}
$\overline{WE}$ Capacitance	C_{WE}			7	pF	V_{IN} = V_{SS}
CE Capacitance	C_{CE1}			27	pF	V_{IN} = V_{SS}
	C_{CE2}			22	pF	V_{IN} = V_{DD}

READ CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Time Between Refresh	t_{REF}		1		2		2		2	ms	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1TTL Gate V_{ref} = 2.0 or 0.8 Volts
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
Cycle Time	t_{CY}	800		470		430		400		ns	
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	ns	
CE Output Delay	t_{CO}		330		280		230		180	ns	
Access Time	t_{ACC}		350		300		250		200	ns	
CE to $\overline{WE}$	t_{WL}	40		40		40		40		ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		ns	

WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ±10%, V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise noted.

PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Cycle Time	t_{CY}	800		470		430		400		ns	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = ITTL Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
CE on Time	t_{CE}	380	3000	300	3000	260	3000	230	3000	ns	
$\overline{WE}$ to CE off	t_W	200		180		180		150		ns	
CE to $\overline{WE}$	t_{CW}	380		300		260		230		ns	
D_{IN} to $\overline{WE}$ Set Up ①	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		40		ns	
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		ns	

Note: ① If $\overline{WE}$ is low before CE goes high then D_{IN} must be valid when CE goes high.

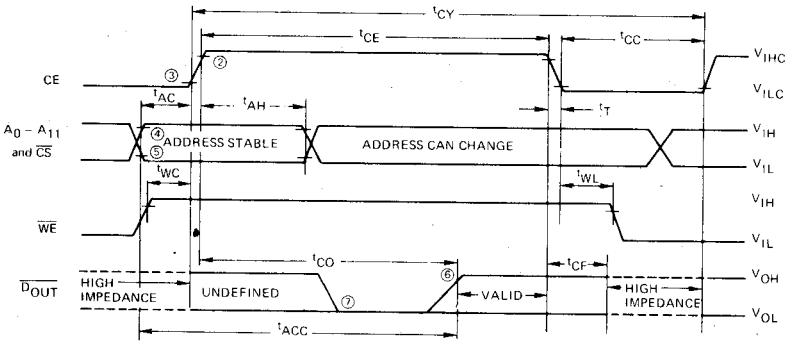
READ-MODIFY-WRITE CYCLE

T_a = 0°C to 70°C, V_{DD} = 12V ± 10%, V_{CC} = 5V ± 10%, V_{BB} = -5V ± 10%, V_{SS} = 0V, unless otherwise noted.

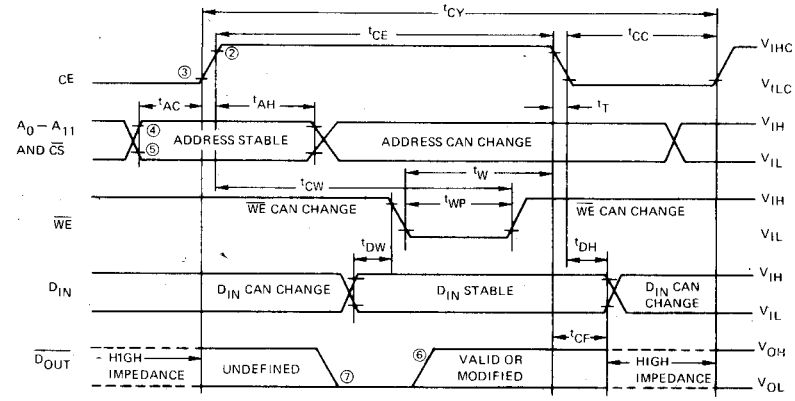
PARAMETER	SYMBOL	LIMITS μPD411A-E MIN	μPD411A-E MAX	μPD411A MIN	μPD411A MAX	μPD411A-1 MIN	μPD411A-1 MAX	μPD411A-2 MIN	μPD411A-2 MAX	UNIT	TEST CONDITIONS
Read-Modify-Write (RMW) Cycle Time	t_{RWC}	960		650		600		520		ns	$t_T = t_r = t_f$ = 20 ns C_L = 50 pF Load = 1TTL Gate V_{ref} = 2.0 or 0.8 Volts
Time Between Refresh	t_{REF}		1		2		2		2	ms	
Address to CE Set Up Time	t_{AC}	0		0		0		0		ns	
Address Hold Time	t_{AH}	150		150		150		150		ns	
CE Off Time	t_{CC}	380		130		130		130		ns	
CE Transition Time	t_T	0	40	0	40	0	40	0	40	ns	
CE Off to Output High Impedance State	t_{CF}	0	130	0	130	0	130	0	130	ns	
CE Width During RMW	t_{CRW}	540	3000	480	3000	430	3000	350	3000	ns	
$\overline{WE}$ to CE on	t_{WC}	0		0		0		0		ns	
$\overline{WE}$ to CE off	t_W	200		180		180		150		ns	
$\overline{WE}$ Pulse Width	t_{WP}	200		180		180		150		ns	
D_{IN} to $\overline{WE}$ Set Up	t_{DW}	0		0		0		0		ns	
D_{IN} Hold Time	t_{DH}	40		40		40		40		ns	
CE to Output Delay	t_{CO}		330		280		230		180	ns	
Access Time	t_{ACC}		350		300		250		200	ns	

TIMING WAVEFORMS

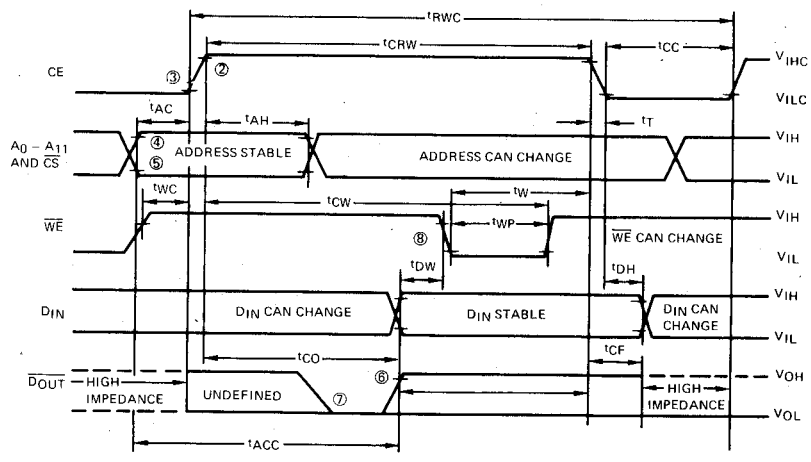
READ AND REFRESH CYCLE ①



WRITE CYCLE



READ-MODIFY-WRITE CYCLE



Notes:

① For refresh cycle, row and column addresses must be stable t_{AC} and remain stable for entire t_{AH} period.

② V_{DD} – 2V is the reference level for measuring timing of CE.

③ V_{SS} + 2V is the reference level for measuring timing of CE.

④ V_{IHMIN} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

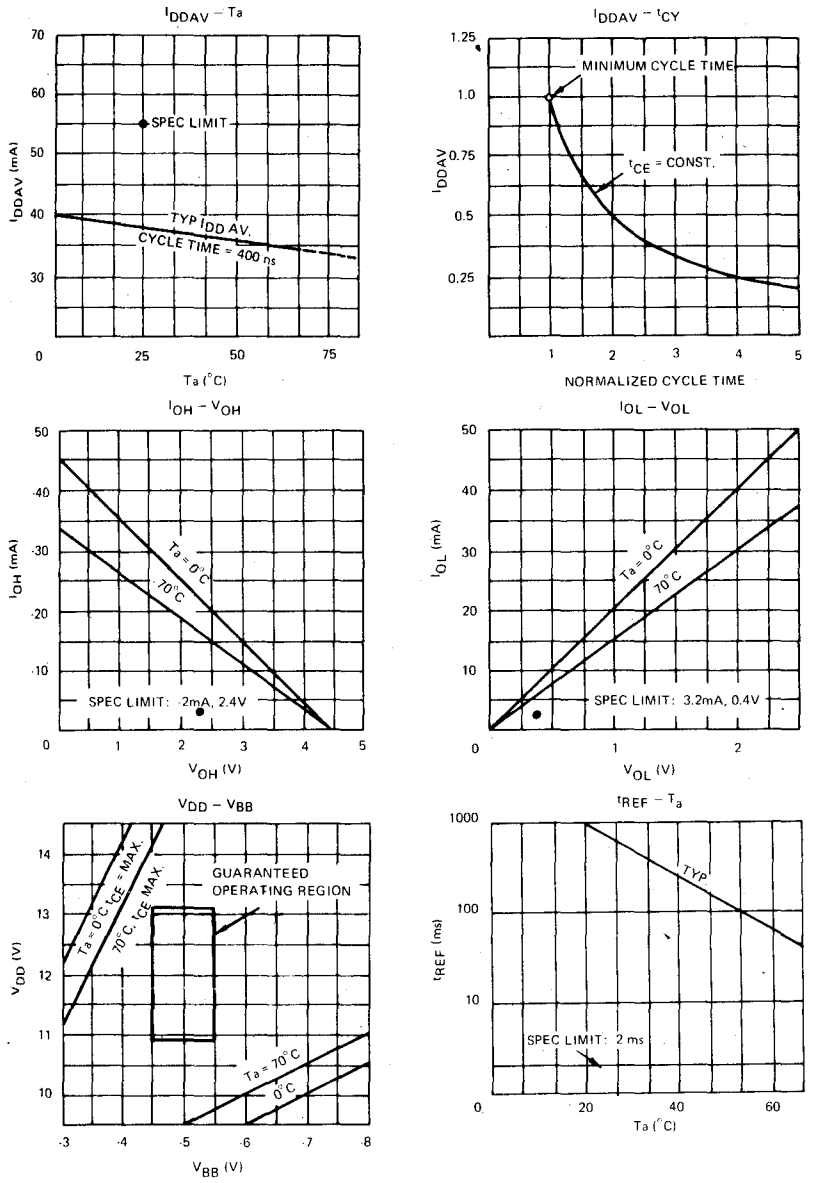
⑤ V_{ILMAX} is the reference level for measuring timing of the addresses, $\overline{CS}$, $\overline{WE}$ and D_{IN}.

⑥ V_{SS} + 2.0V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑦ V_{SS} + 0.8V is the reference level for measuring timing of $\overline{D_{OUT}}$.

⑧ $\overline{WE}$ must be at V_{IH} until end of t_{CO}.

TYPICAL OPERATING CHARACTERISTICS



POWER CONSUMPTION

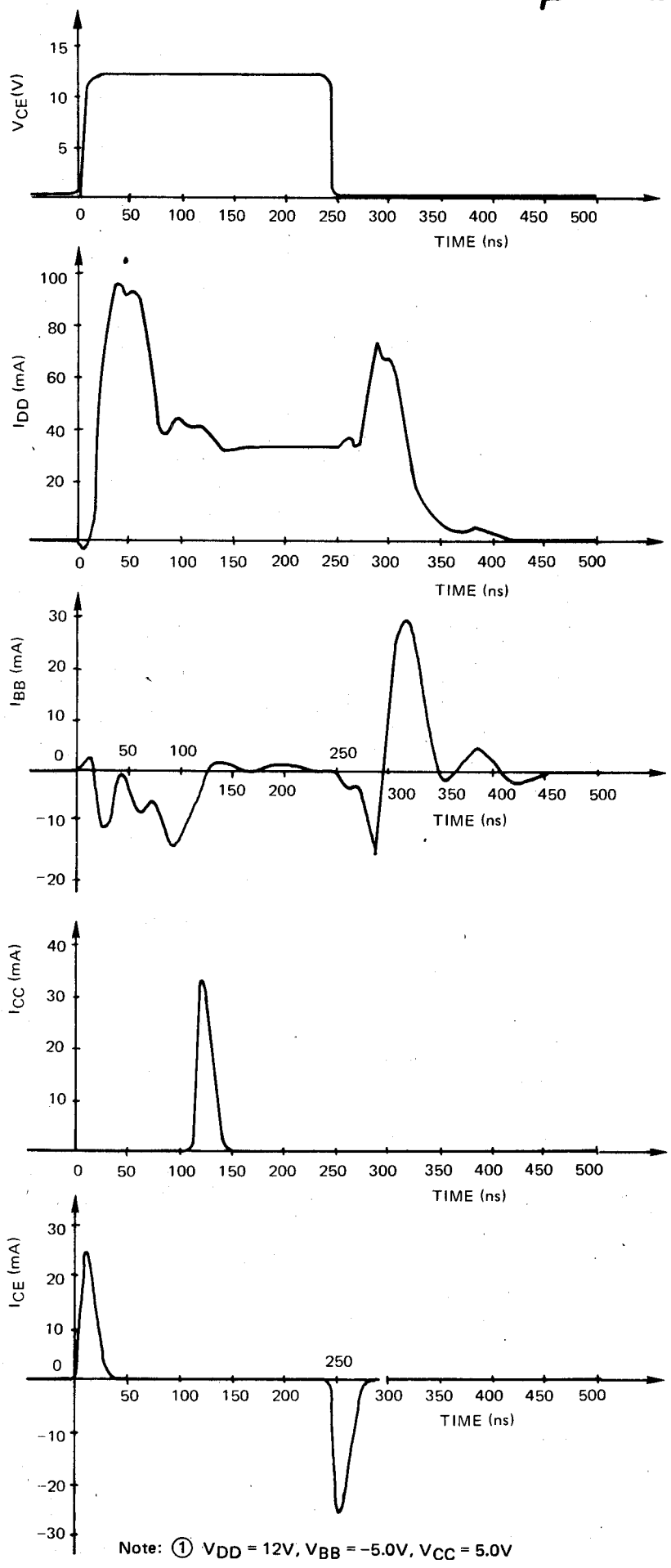
Power consumption = $V_{DD} \times I_{DDAV} + V_{BB} \times I_{BB}$

Typical power dissipation for each product is shown below.

	mW (TYP.)	CONDITIONS
μPD411A-E	300 mW	$T_a = 25°C$, $t_{cy} = 800$ ns, $t_{CE} = 380$ ns
μPD411A	460 mW	$T_a = 25°C$, $t_{cy} = 470$ ns, $t_{CE} = 300$ ns
μPD411A-1	460 mW	$T_a = 25°C$, $t_{cy} = 430$ ns, $t_{CE} = 260$ ns
μPD411A-2	460 mW	$T_a = 25°C$, $t_{cy} = 400$ ns, $t_{CE} = 230$ ns

See curve above for power dissipation versus cycle time.

CURRENT WAVEFORMS ①



Note: ① V_{DD} = 12V, V_{BB} = −5.0V, V_{CC} = 5.0V